



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Prashanth Bhat et al. Examiner: Shah, Nilesh R.
Application No. : 09/865,988 Group Art Unit: 2127
Filing Date : May 25, 2001
Art Unit : 2127
Title : LOAD BALANCING SYSTEM AND METHOD IN A
MULTIPROCESSOR SYSTEM

Commissioner for Patents
PO Box 1450
Alexandria VA 22313-1450

Communication Pursuant to Rule 116

Sir:

In response to the Office Action dated April 15, 2005, please reconsider the above-identified application in light of the following:

Claims begin on page 2 of this paper.

Remarks begin on page 11 of this paper.

*Enter with PRA
Chaitis
2/16/06
12/13/05*